Amendments to Specification

Amend the paragraph starting at page 4, line 11 as follows:

The device according to the present invention for analyzing digital data, as shown in Fig. 2, adds further components to the general architecture shown in Fig. 1. The microprogram in a microprogram memory is now referenced as a microcode memory **18** which contains information on at least one communication protocol to be decoded. Particularly a tree of rules describing the protocol is represented as a microcode in the microcode memory **18**. Via an input **20** the microcode memory **18** may be reloaded with other protocols and/or further needed parts of a protocol not fully loaded. This microcode memory **18** is accessed for reading only. The content of a microcode or control register **22** may be newly loaded with a clock **24**. Via an input **25** the protocol data units (PDUs) to be analyzed are loaded into a data memory **26**. From there the data are loaded into a data register **28** for analysis. Since the data to be analyzed may be contained in the data memory **26** across two address lines, the data register **28** is designed to shift and align the data read in. The data memory **26** also is accessed for reading only. The analysis results are entered into an output memory **30** that makes the results available at an output **32** to other units for further processing. A register block **36** has several registers and counters, the contents of which impact on subsequent addresses in the data memory **26** and/or microcode memory **18**. For example a register PDU_LEN may contain the length of a PDU just analyzed in the data register **28**, or a part thereof, so that once the desired parameter is found it is possible with knowledge of the length of the PDU to directly read out the next PDU from the ~~dat~~ data memory **26**. In

a similar way a PARAM_LEN register may serve to jump directly to the next parameter after a parameter has been found, provided that this follows from the parameter, while a SEQ_CNT register may serve to increase or decrease the addressed by predetermined values.

Amend the paragraph starting at page 9, line 8 as follows:

In the preferred embodiment the first and second addressing units **34, 40** each contain at least one counter that may be modified in accordance with the content of the data register **28** and/or the microcode register **22** when the addresses are determined. This makes it possible to jump straight to subsequent addresses in the respective memories **26, 18**, depending on the relevant register contents. The data register **28** is preferably designed such that its content may be aligned or shifted. This makes it possible to reliably analyze even data in PDUs that extend across two addresses, such as from the end of a first address to the beginning of a second address. The register block **36** takes account of the contents of the data register **28** and/or the microcode register **22** of preceding ~~pints~~ points in time, which are decisive for the addresses. If a PDU extends across several addresses and the parameter searched for has already been found, it is possible from the length of the relevant PDU filed in the register block **36** to jump directly to the next address of interest which indicates the beginning of the next PDU. The third addressing unit **46**, having a changeable address and taking the content of the microcode register **22** into account, allows writing the results not only serially into the output memory **30**, but already in a form that is particularly advantageous for further processing, such as first a list of the parameter identifiers and then a list of the associated parameter

values. In case the content of the output memory **30** is updated in steps, and existing line entries in particular are updated in respect of new analyzing results, it is particularly advantageous for the device to have the logic circuit **50** with which an entry of the output memory is read out, changed to take account of the new result, and rewritten into the output memory. For the start of an analysis in which a higher level system may define the entry address into the microprogram, it is particularly advantageous that the addressing units **34, 40, 46** are designed such that a starting address may be loaded into them. At least two of the memories **18, 26, 30** may be combined in one physical memory, and the associated addressing units **34, 40, 46** also may be combined into a single physical addressing unit.